

FIG.1
PRIOR ART

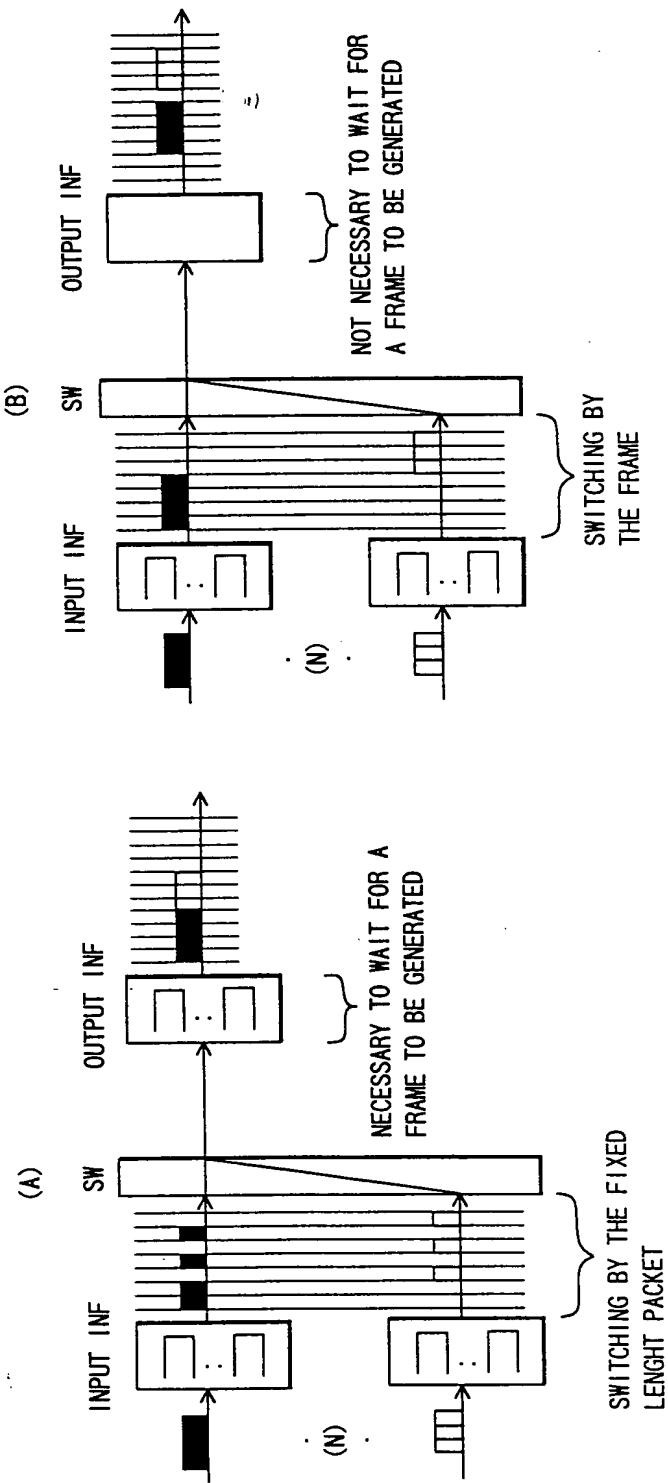


FIG.2

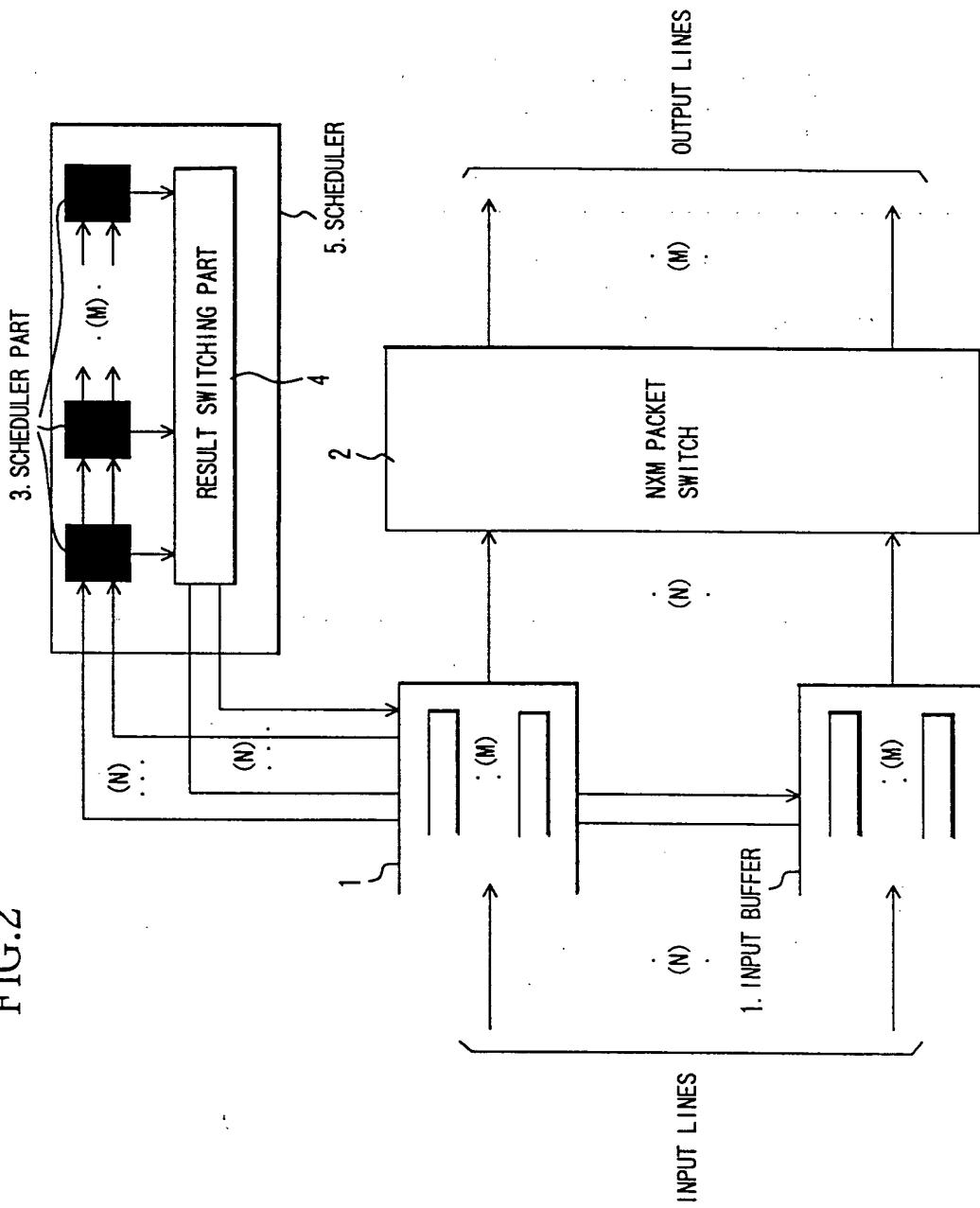


FIG.3

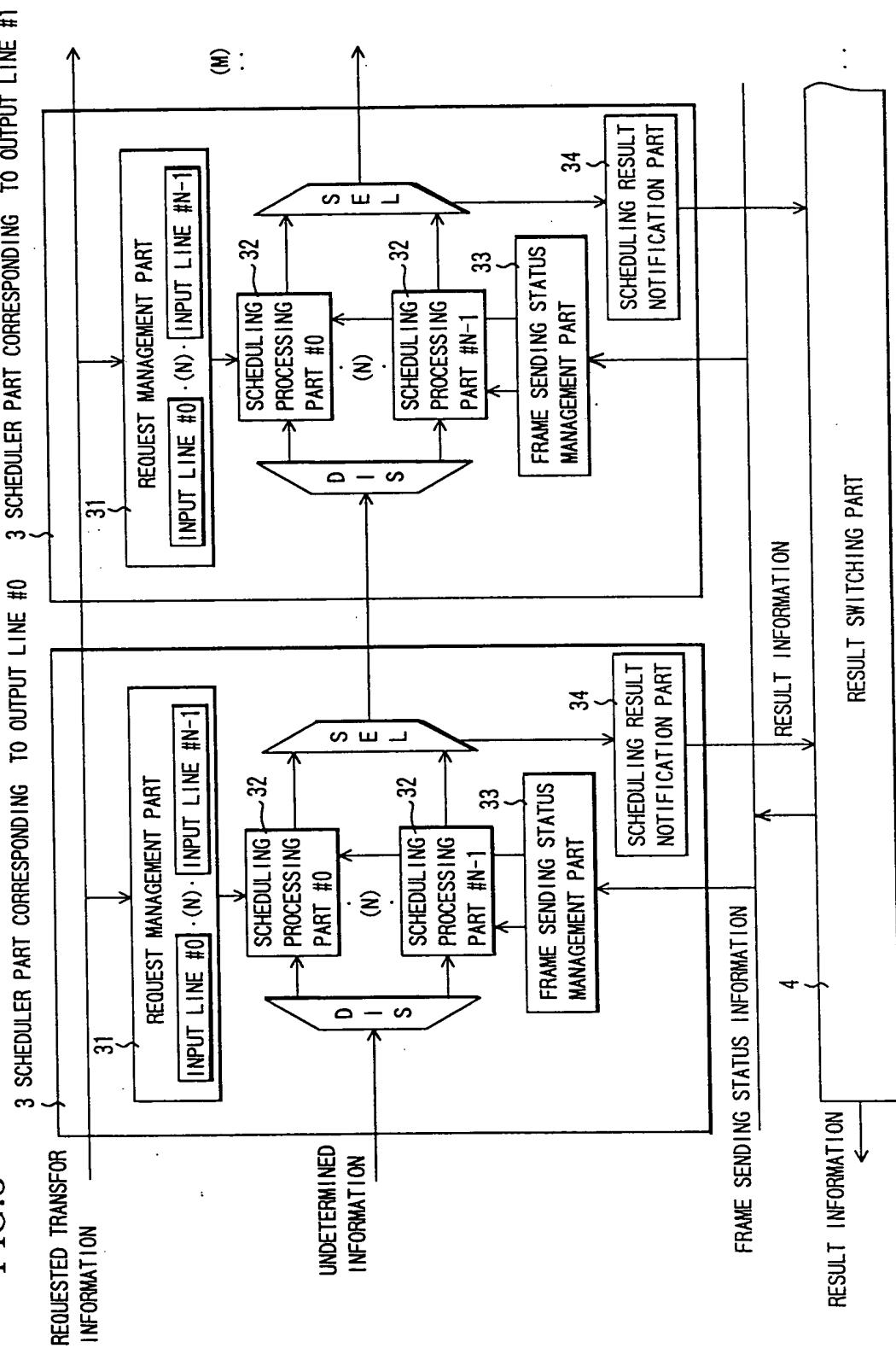
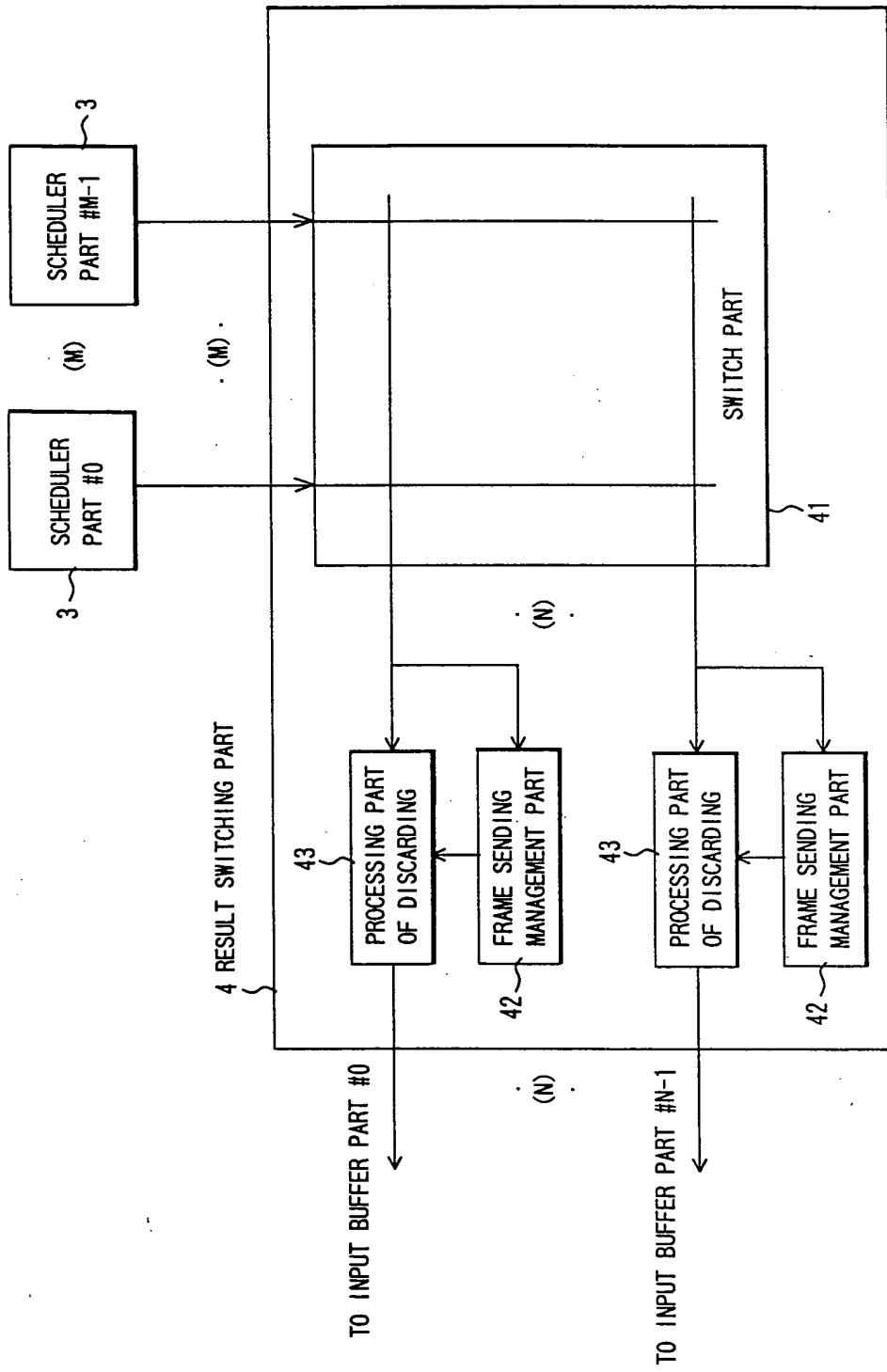


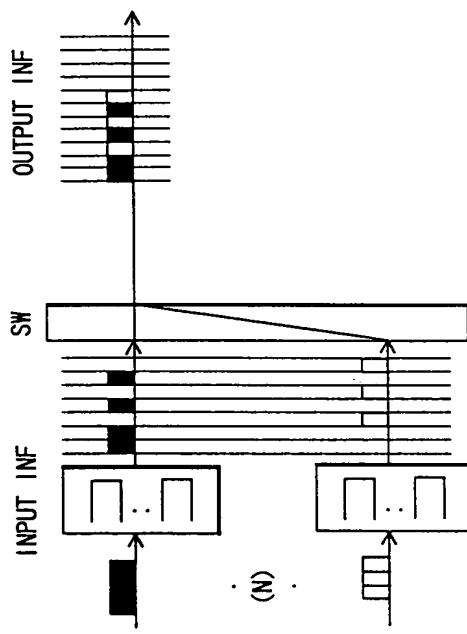
FIG.4



प्र० अ० व० व० व० व० व०

FIG.5

(A) CASE WHERE FRAMES ARE NOT CONSIDERED



(B) CASE WHERE FRAMES ARE CONSIDERED

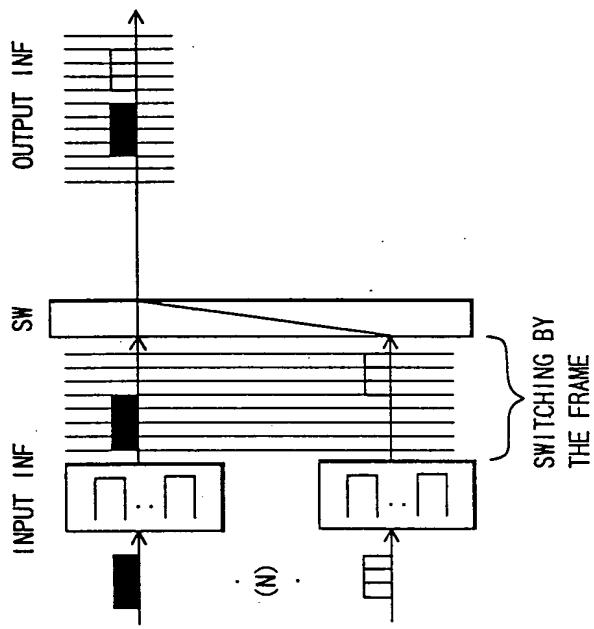


FIG.6

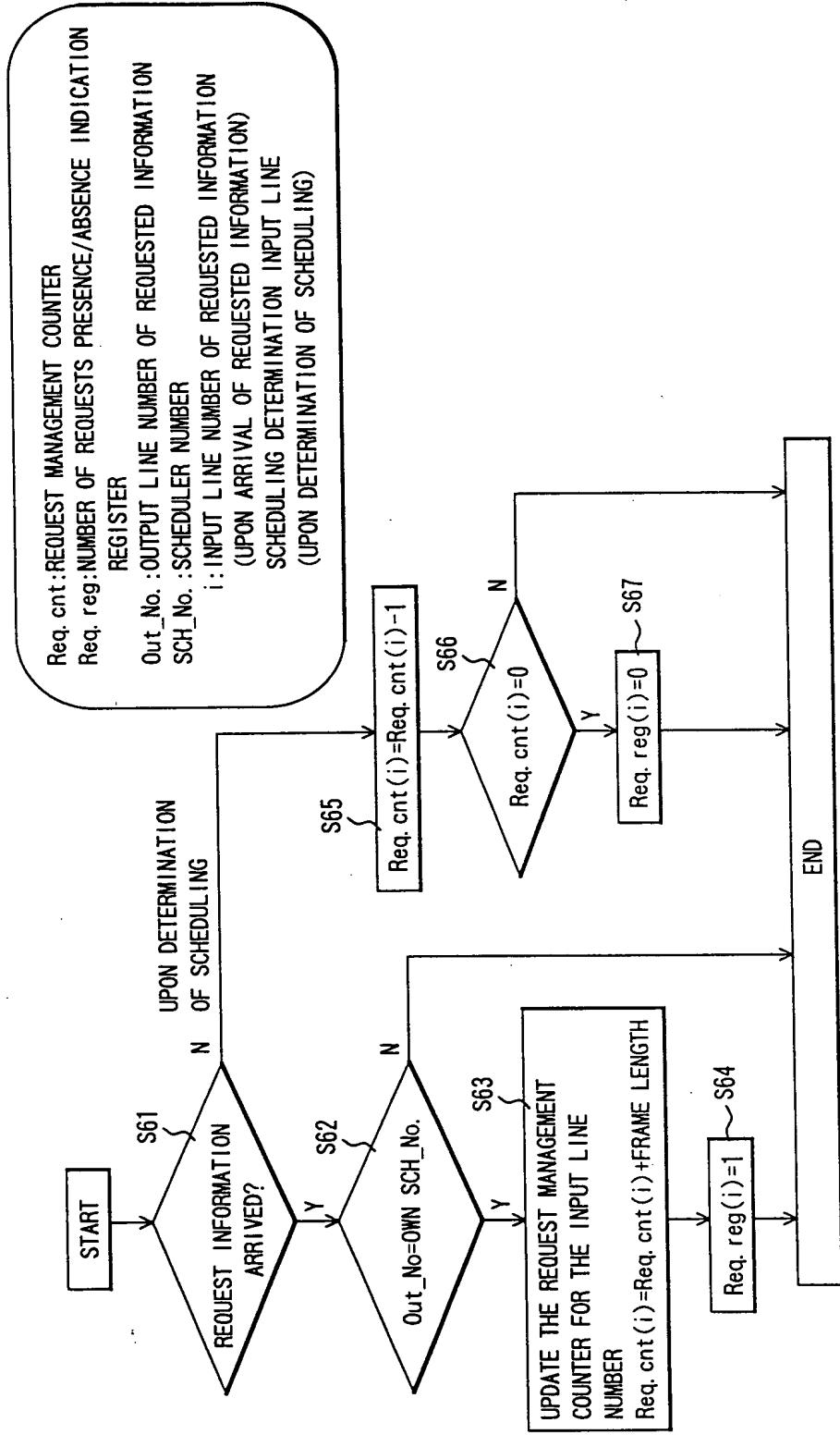


FIG.7

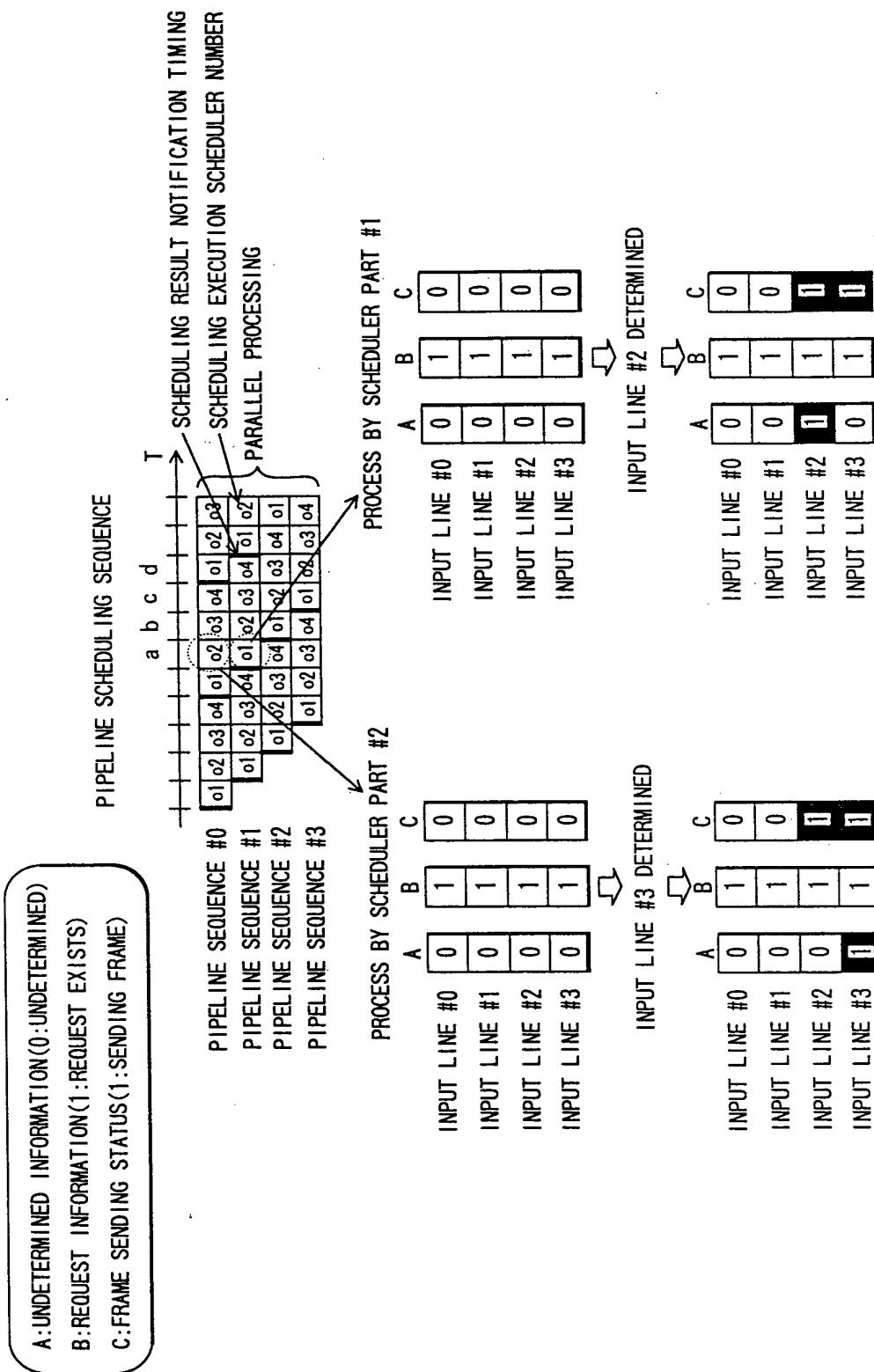


FIG.8

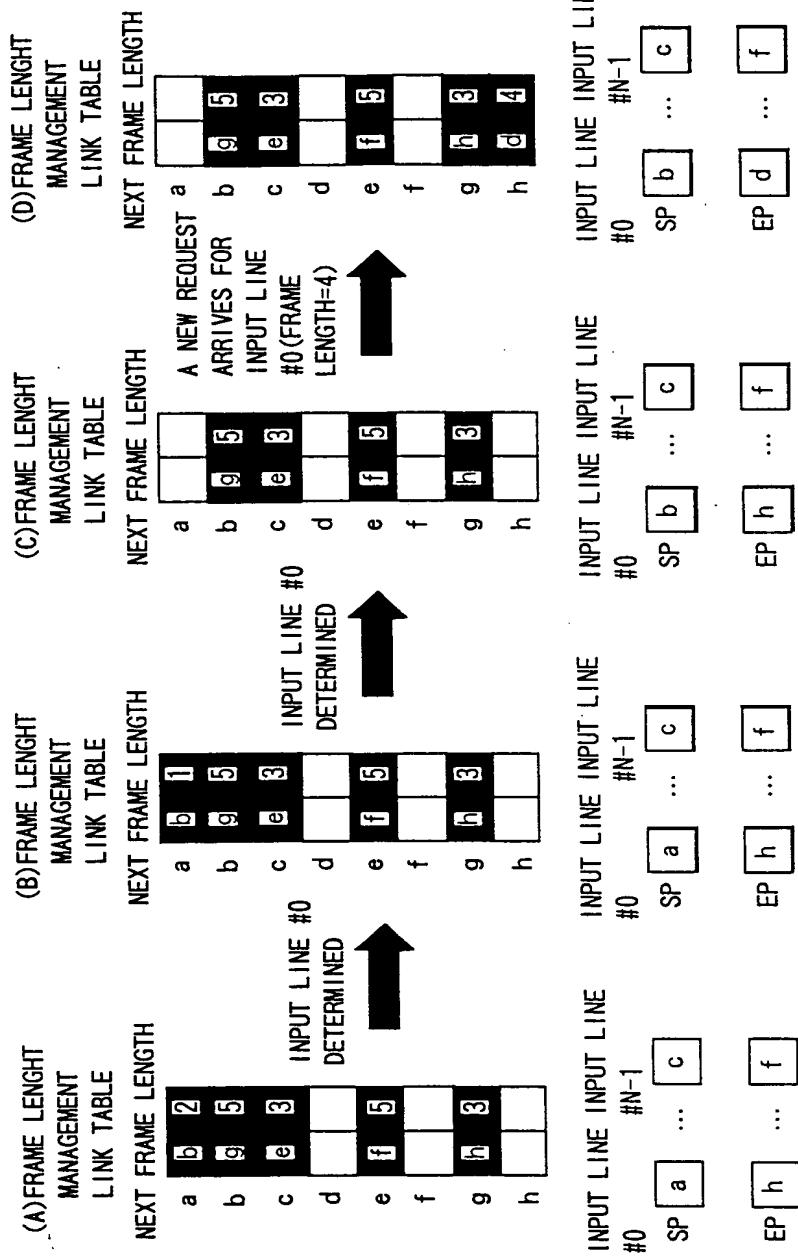


FIG.9

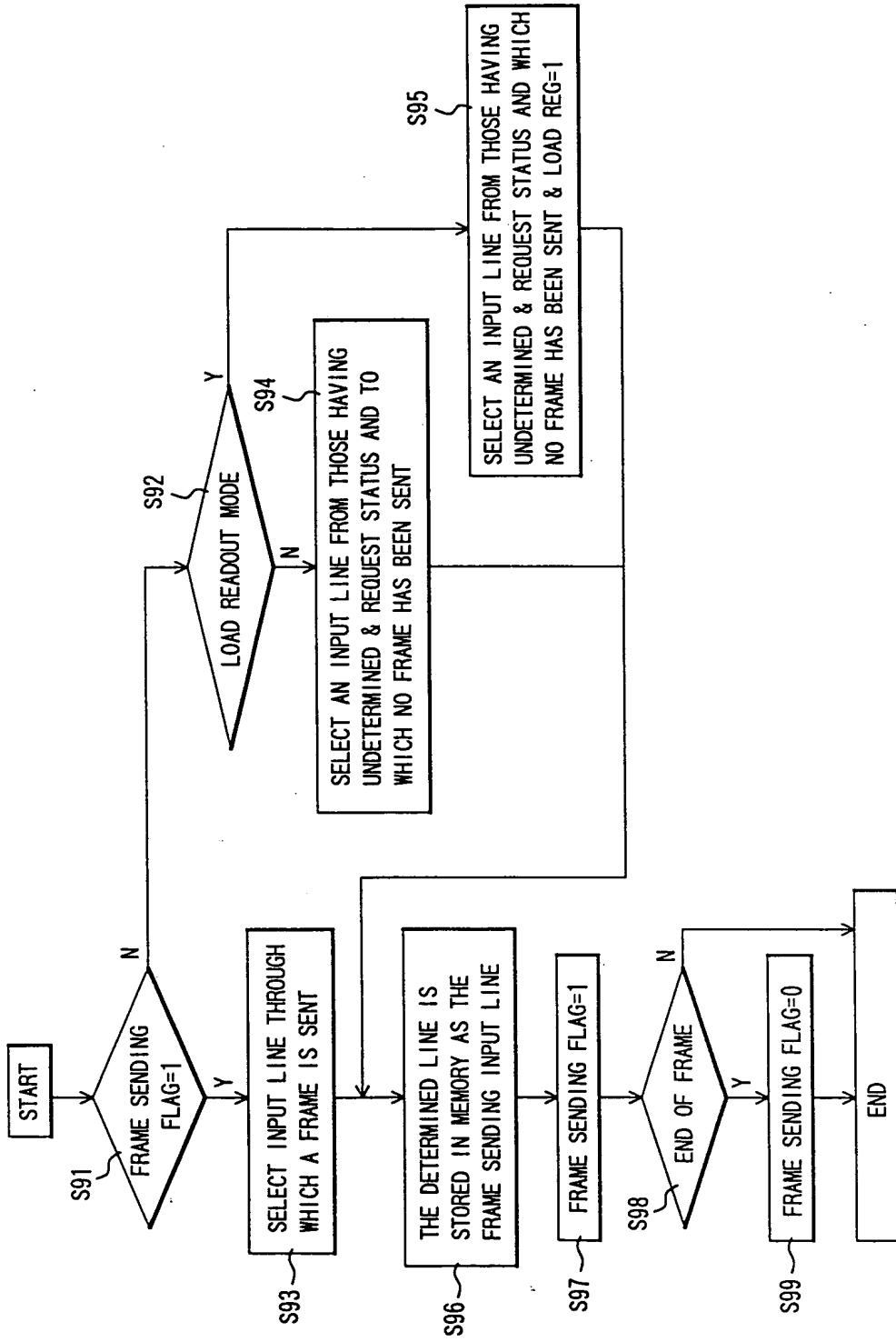


FIG. 10

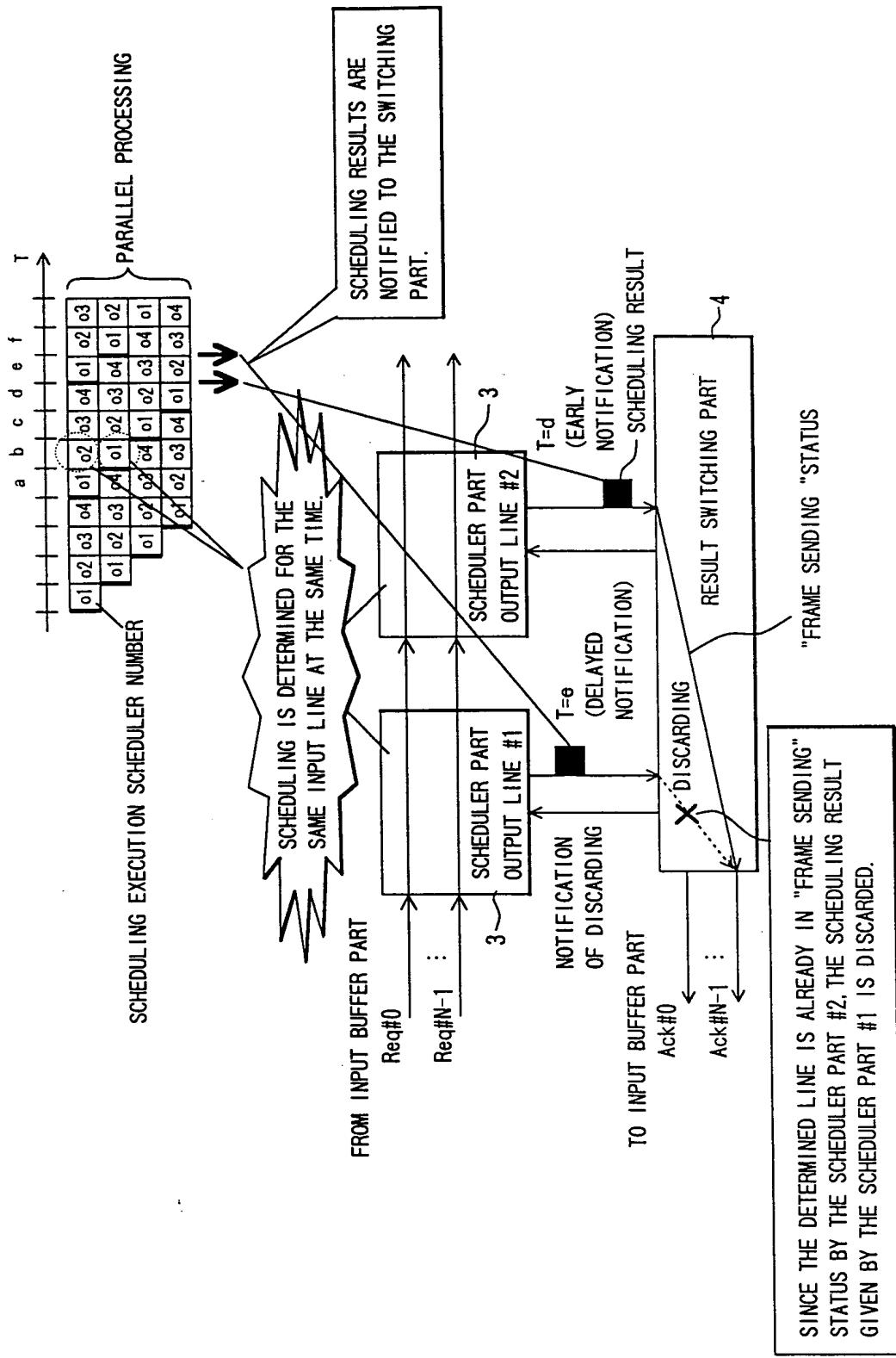
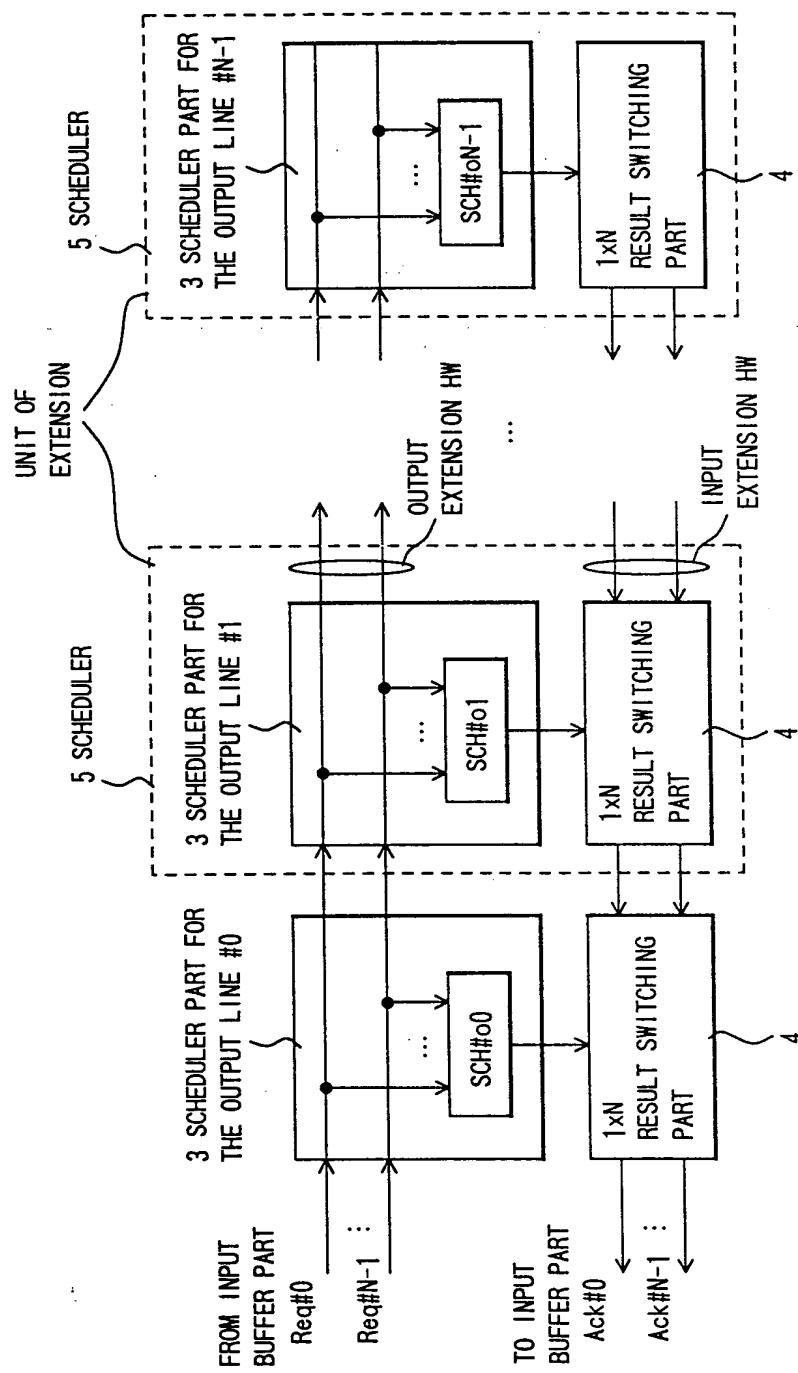


图 6.2.2 为图 6.2.1 的具体实现

FIG.11



FROM INPUT
BUFFER PART

Req#N-1 :
Req#0

FIG.12

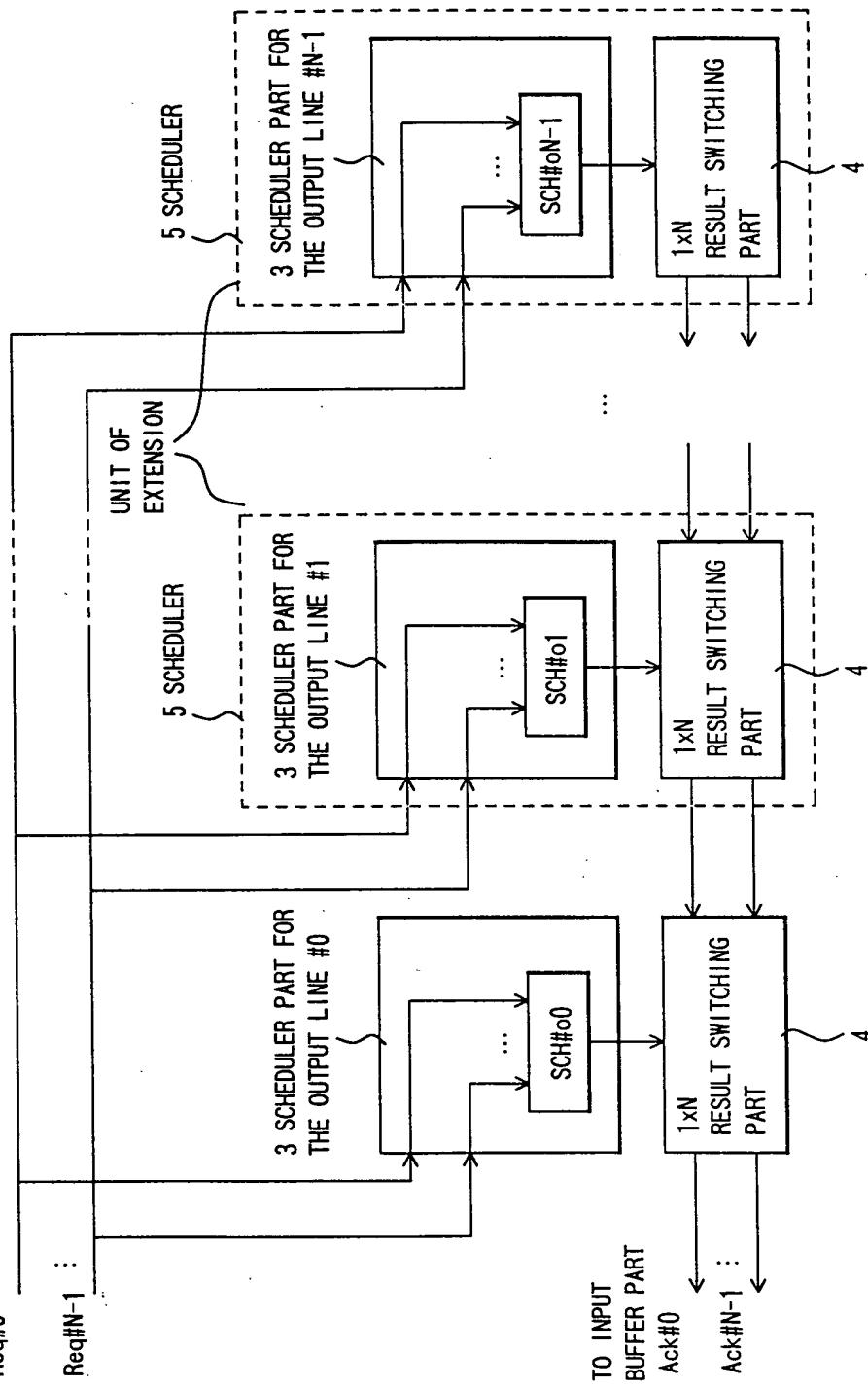


图 3.22 图 3.23 图 3.24 图 3.25

FIG.13

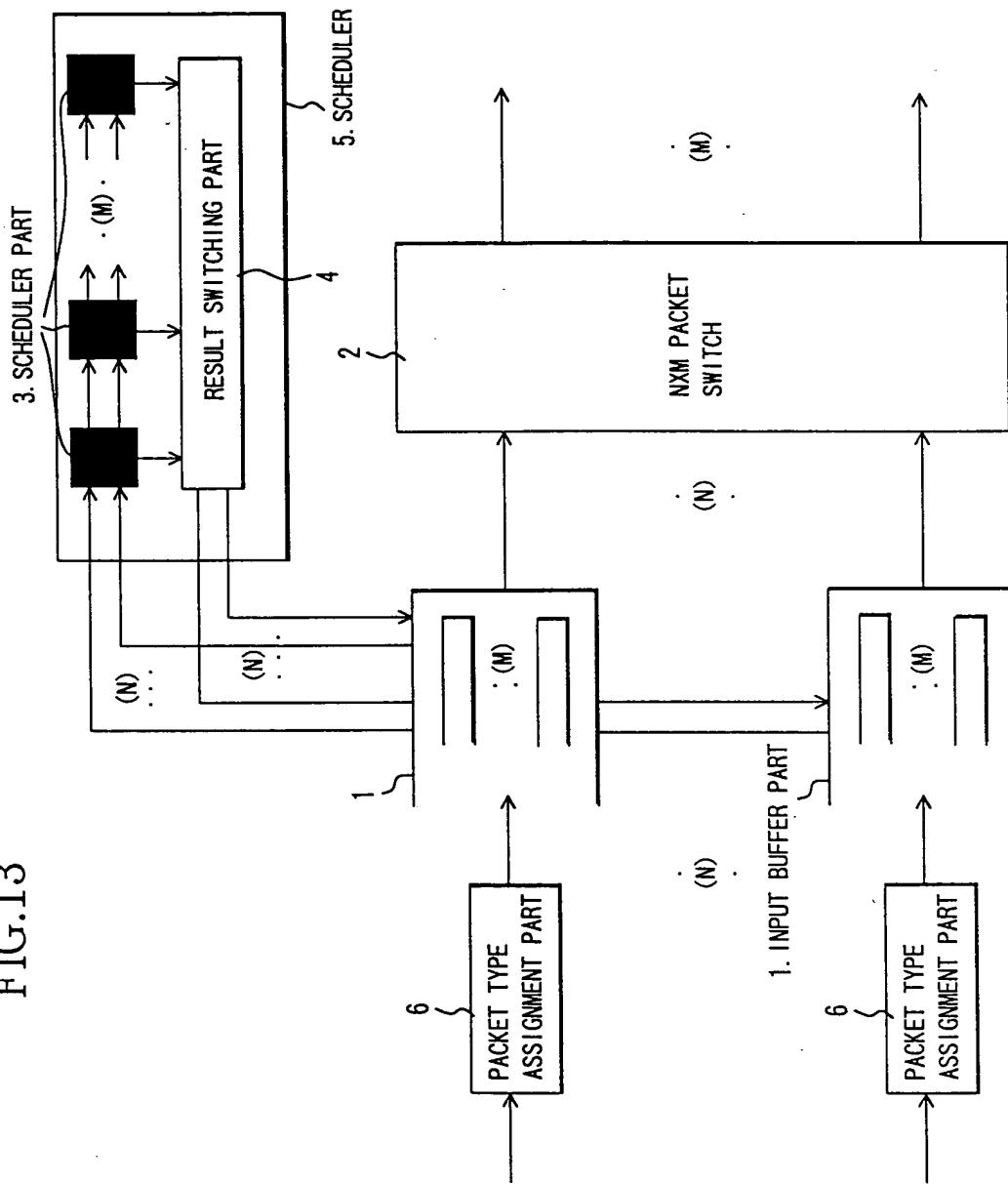
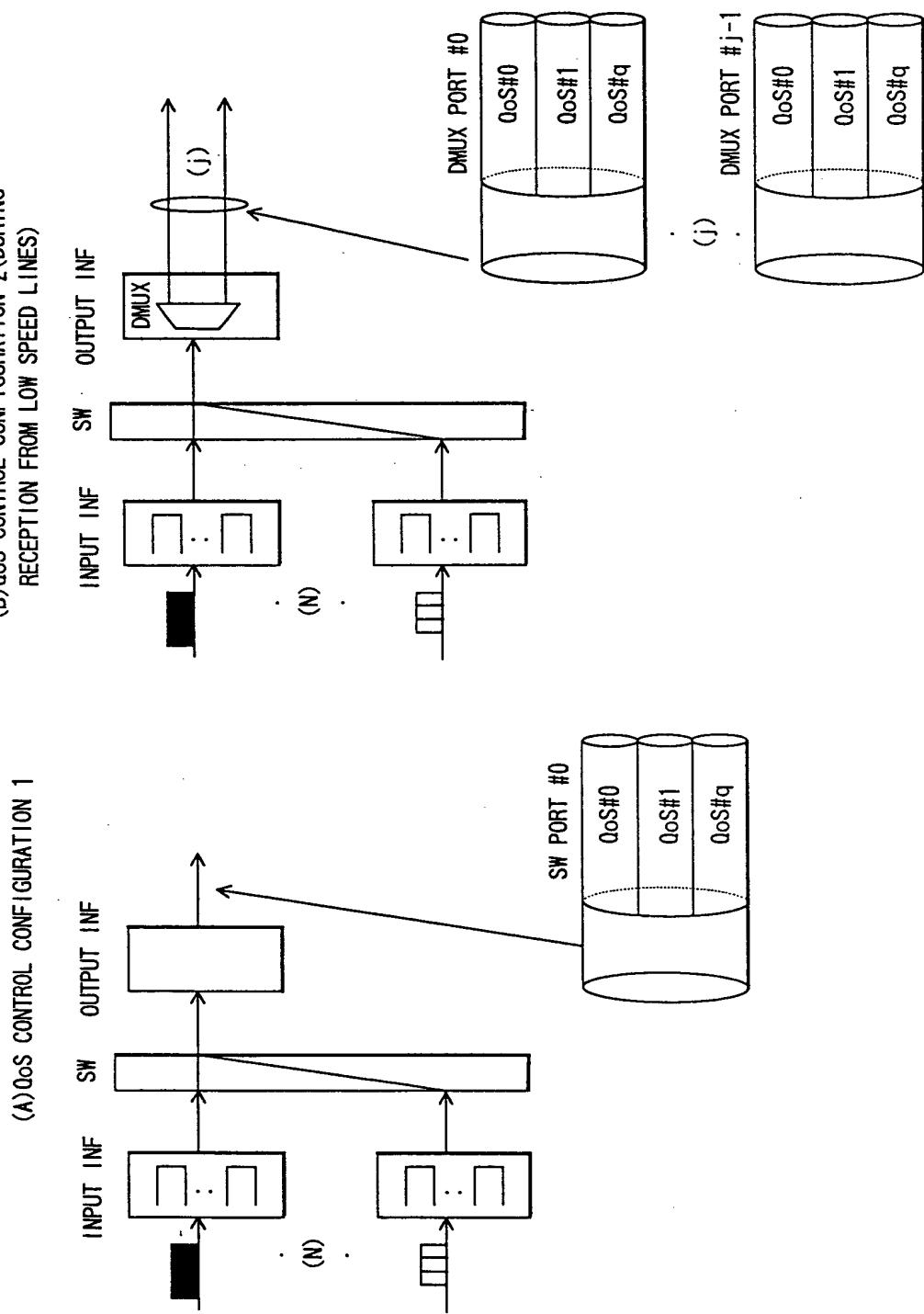
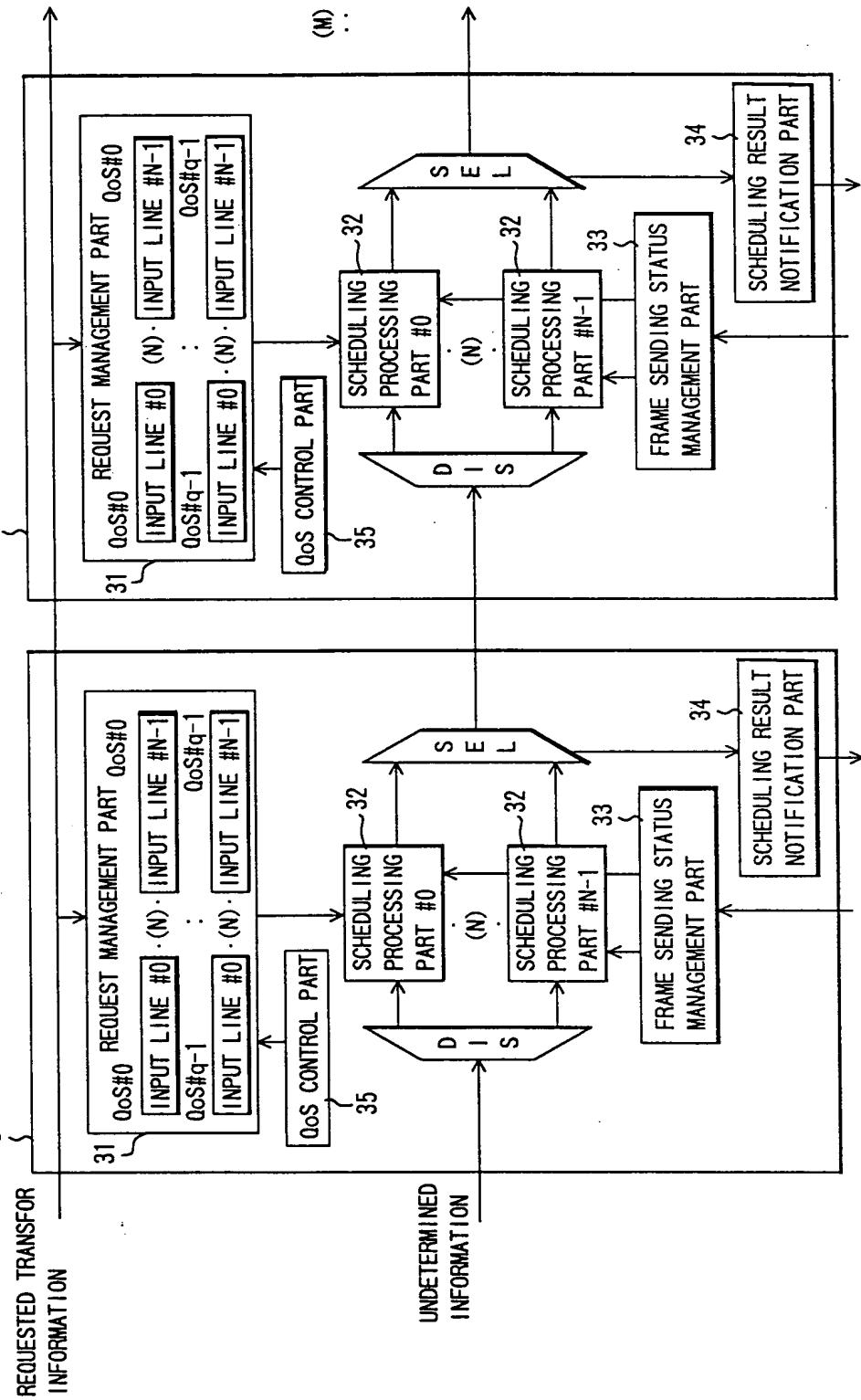


FIG.14



UNDETERMINED INFORMATION

FIG.15 3 SCHEDULER PART CORRESPONDING TO OUTPUT LINE #0 3 SCHEDULER PART CORRESPONDING TO OUTPUT LINE #1



T024 T025 T026 T027 T028

FIG.16

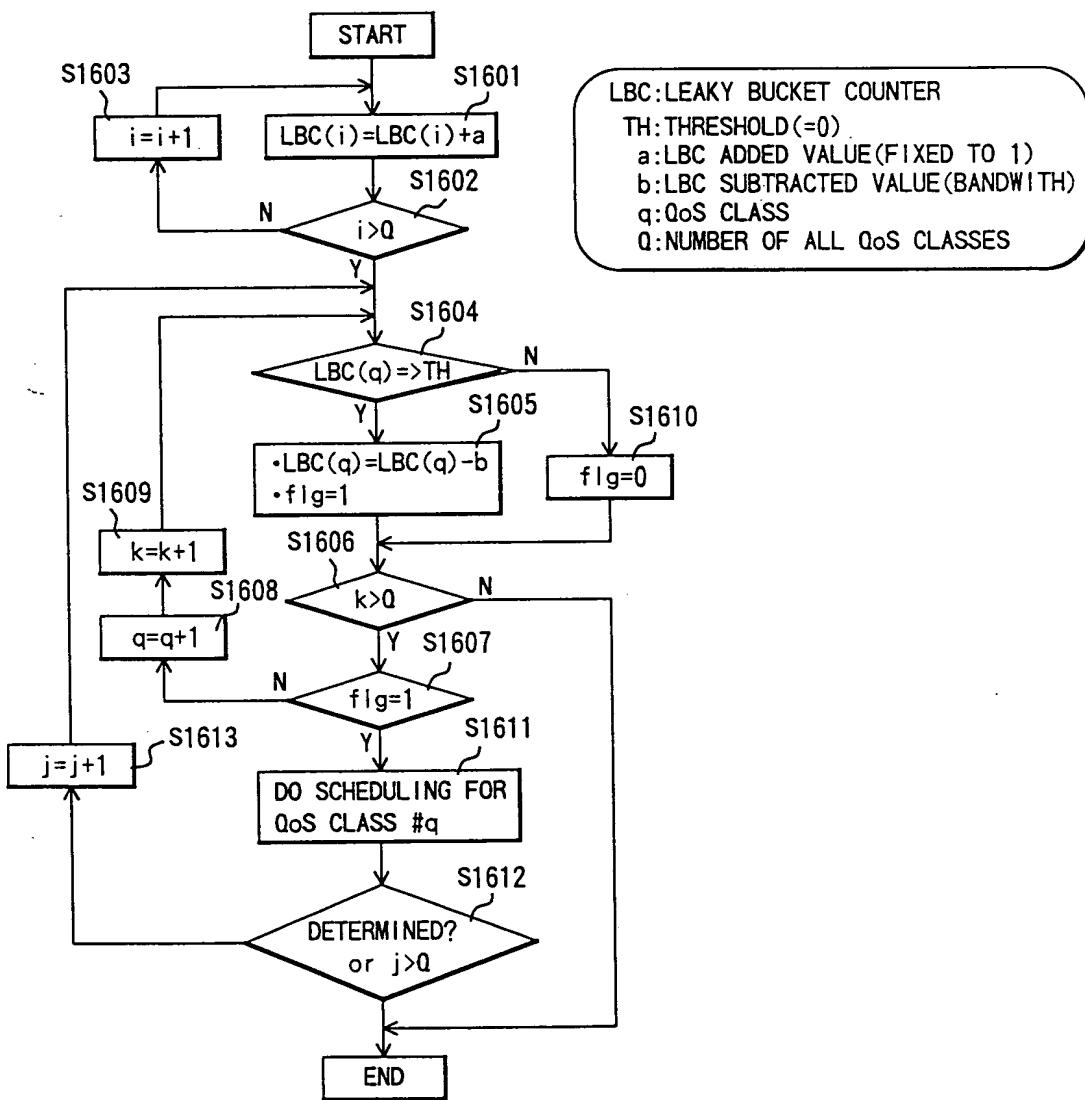
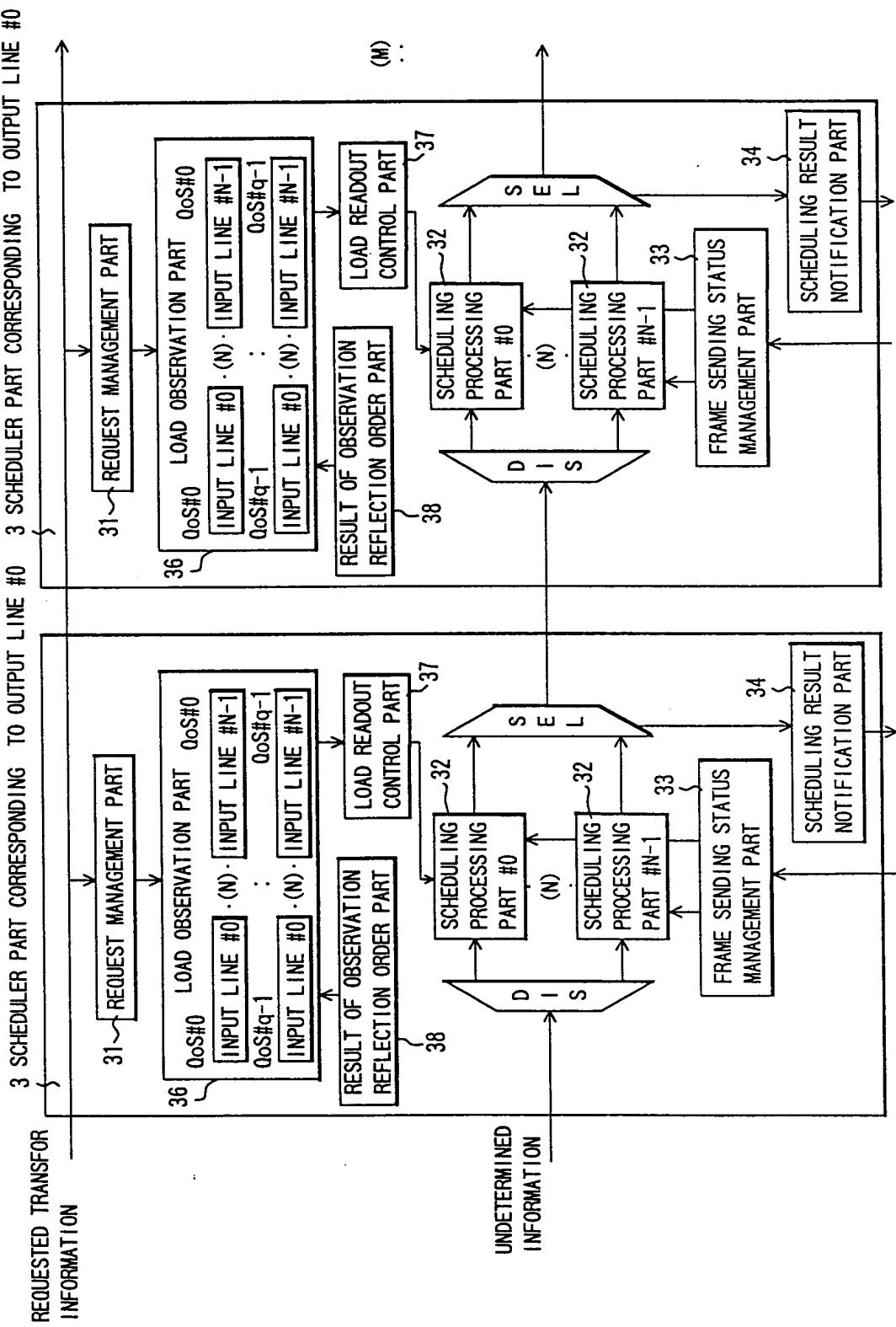


FIG. 17



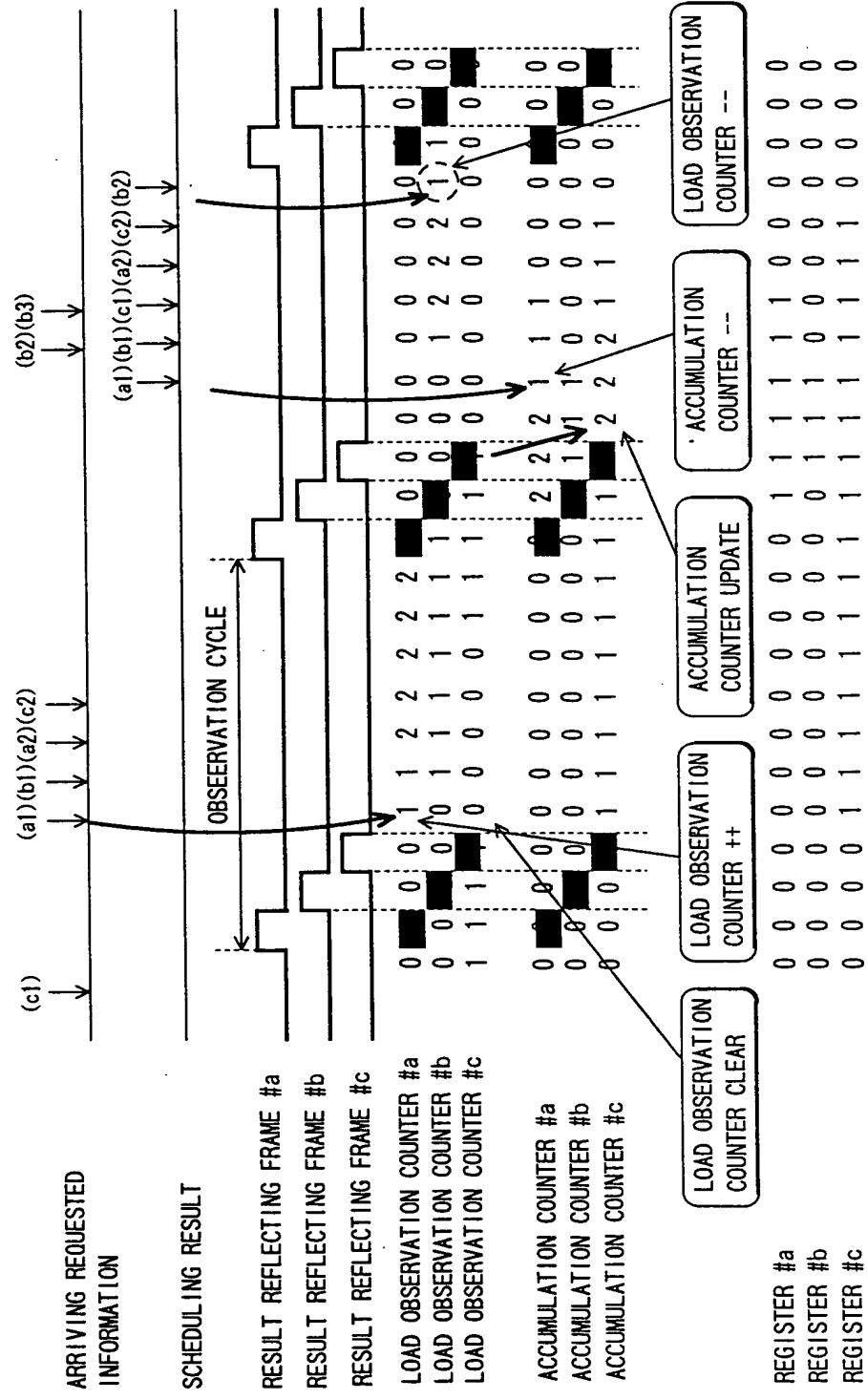


FIG. 19

